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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Use several sheets if necessary)		APPLICANT TAKASE, et al.	10/042351 S-1 10/042351 S-1 10/042351 S-1
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U.S. PATENT DOCUMENTS

Examiner Initial	Document Number	Date	Name	Class	Subclass	Filing Date
AA						
AB						
AC						
AD						
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AF						
AG						

FOREIGN PATENT DOCUMENTS

Examiner Initial		Document Number	Date	Country	Class	Subclass	Translation	
							Yes	No
MS4	AM	2000-78148	2000	Japan				
	AN							
	AO							
	AP							
	AQ							
	AR							
.	AS							
	AT							

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

M9A	AU	"Improvement for Packet Priority of the Packet Switch with Multiple Input Queues for Every Output Port"; TAKAJYO; Technical Report of IEICE. SSE97-13, IN97-13(1997-04); pages 37-43
M9A	AV	"A Study on the Architecture of Large Scale Packet Switching System"; WAKAYAMA; Technical Report of IEICE. SSE98-160, PS98-50(1998-12); pages 67-72
M9A	AW	"A Study of Input-buffer Switch Scheduling"; SUDO, Technical Report of IEICE. SSE99-118, PS99-42(1999-12); pages 43-48
M9A	AX	"Proposal and Performance Evaluation of a Queue Length Based Weighted Fair Queueing Algorithm"; OHBA; Technical Report of IEICE. SSE96-56(1996-08); pages 79-84
	AY	
	AZ	

Examiner

Date Considered

10/21/2005